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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,478	11/01/2001	Craig Nemecek	CYPR-CD01213M	6435

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EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 05/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,478	NEMECEK ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-21 have been presented for examination. Claims 1-21 have been rejected.

Priority

1. This Application contains a claim for the benefit of priority to U.S. Provisional Application No. 60/243,708 filed 26 October 2000. The provisional application has been reviewed and priority is denied, because the provisional application does not appear to enable the claimed invention as required under 35 U.S.C. Section 112, first paragraph. See 35 U.S.C. § 119(e)(1).

For example, the provisional application contains a set of 'powerpoint-style' drawings and datasheets describing desired features for a microcontroller or a 'system-on-chip,' but this material does not appear to contain either the text description or the drawings found in the Application. In particular, no part of the provisional application appears to disclose the method steps shown in the Application at Fig. 7.

Technology Background

In the interests of facilitating a discussion of the prior art, the Examiner provides the following concepts and definitions as known in the art.

The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition (2000) provides the following definitions:

- **parallelism (A)** Concurrent operations of several parts of a computer system. *Note:* This could be simultaneous processing of multiple programs, or simultaneous operation of multiple computers. **(B)** Pertaining to specific techniques for implementing parallel operations. *See also:* AND-parallelism; OR-parallelism.
- **AND-parallelism** Pertaining to the performance of multiple predicate operations concurrently; the successful completion of which results in a true response.
- **concurrent execution** Functions that suspend the execution of the calling thread shall not cause the execution of other threads to be indefinitely suspended.
- **concurrent processes (software)** Processes that may execute in parallel on multiple processors or asynchronously on a single processor. Concurrent processes may interact with each other, and one process may suspend execution pending receipt of information from another process or the occurrence of an external event. *See also:* sequential processes; execution.
- **breakpoint (1) (A) (computer routine)** Pertaining to a type of instruction, instruction digit, or other condition used to interrupt or stop a computer at a particular place in a routine when manually requested. **(B) (computer routine)** A place in a routine where such an interruption occurs or can be made to occur. **(2) (software)** A point in a computer program at which execution can be suspended to permit manual or automated monitoring of program performance or results. Types include code breakpoint, data breakpoint, dynamic breakpoint,

epilog breakpoint, programmable breakpoint, prolog breakpoint, static breakpoint. *Note:* A breakpoint is said to be set when both a point in the program and an event that will cause suspension of execution at that point are defined; it is said to be initiated when program execution is suspended. **(3)** A position within a pattern set where the pattern may be segmented into multiple independent bursts while still achieving predictable behavior of the device.

- **breakpoint instruction (A)** A computer instruction that causes program flow to be halted. *See also:* address stop. **(B)** A computer instruction that causes program flow to be redirected to a monitor or debugging system. *Synonym:* breakpoint halt; dynamic stop.
- **address stop** An address that, when it is encountered by a program, causes the program to halt execution. *See also:* breakpoint instruction; instruction address stop.
- **register (4)** A storage device or storage location having a specified storage capacity.

Claim Objections

2. Applicant is advised that should claim 2 (or claim 13) be found allowable, claim 3 (14) will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after

allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

This warning is applied in light of the definition of "register", supplied above, as known in the art. The terms "memory" and "register" are generally synonymous, however specialized forms of either could be distinguished from each other. If Applicant believes the disclosure adequately distinguishes between the term "register" and "memory", clarification is respectfully requested.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 6 and 17 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. These claims recite the phrase "wherein the boot code is stored within the microcontroller and hidden from the virtual microcontroller". It is unknown what constitutes "hiding code" from a virtual microcontroller. This could mean implementing the virtual microcontroller with means to access the code but refusing to provide the code when requested, implementing the virtual microcontroller with no means to access the code but providing individual instructions as necessary, or implementing the system so that the virtual microcontroller never executes or manipulates the code.

4. Claims 17, 19 and 20 recite the limitations "microcontroller" and "virtual microcontroller" in several locations. There is insufficient antecedent basis for this limitation in the claim. It is presumed that these phrases should be replaced with "device under test" and "virtual processor". Appropriate correction is required.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependency.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,202,044 to Tzori.

Regarding claims 1 and 12, Tzori teaches an emulation system having a microcontroller, effectively the device under test (DUT), operating in lock-step with a virtual microcontroller, effectively a virtual processor (abstract; column 5, lines 14-24). Tzori also teaches a "disengaged mode" (column 5, lines 25-64) wherein the hardware pod (including the microcontroller or DUT) commences execution of instructions without transmitting response data to the simulation process (virtual microcontroller or virtual

processor), and the simulation process commences execution without transmitting additional control data to the hardware pod (column 10, lines 54-65). Tzori also teaches an "engagement message" wherein the disengaged mode is terminated and the simulation process and hardware pod return to lock-step execution (column 5, lines 43-51). Tzori teaches that the disengaged mode and corresponding engagement message may be controlled by either the simulation process or the hardware pod (column 5, lines 52-63).

Therefore the steps of executing a set of boot code is regarded as an obvious detail of implementation as Tzori teaches executing instructions in general. Executing boot instructions instead of instructions in general is not a patentable distinction. Executing "timing code timed to take the same number of clock cycles" is clearly taught by Tzori by virtue of the method performed by the simulation process and hardware pod (Figs. 2 and 3; column 9, line 10 – column 10, line 39 regarding engaged mode; column 10, line 40 – column 11, line 8 regarding disengaged mode; column 11, lines 9-33 regarding the return from disengaged to engaged mode). When disengaging the hardware pod to execute a set of boot code, it would be obvious to a person of ordinary skill in the art that Tzori teaches that the simulation process must execute "timing code timed to take the same number of clock cycles".

Regarding the step of simultaneously halting, this step is well known in the art as a breakpoint for a concurrent process. In this instance, the concurrent processes are executing in parallel on separate devices (virtual microcontroller and microcontroller, or virtual processor and DUT). Tzori's system and method are clearly conducive to this

type of breakpoint, achieved by using the control data during the engaged mode (or invoking the engaged mode if necessary) to simultaneously halt both the microcontroller and virtual microcontroller.

It would have been obvious to a person of ordinary skill in the art to use Tzori's system and method for the particular type of device being designed, whether a microcontroller, a processor, an ASIC, or some other form of integrated circuit logic device. The motivation to do so would be found in the teachings of Tzori as cited above as well as from the nature of the problem to be solved. The combination would be formed according to the teachings of Tzori, where the simulation process and digital logic IC taught by Tzori are modified to correspond to the integrated circuit digital logic device preferred by the designer.

Regarding claims 2, 3, 13 and 14, Tzori teaches transmitting response data from the hardware pod (microcontroller or DUT) to the simulation process (virtual microcontroller or virtual processor) (column 11, lines 23-33). This step allows for the simulation process to perform "some portion of the digital logic simulation that must be completed before the simulation process may re-enter the engaged operating mode". It would be obvious to a person of ordinary skill in the art at the time of Applicants' invention that synchronizing the simulator process and hardware pod is necessary and performed at this step. As synchronization between the two devices means their registers (real or virtual) and memory contents hold the same values, it would be obvious to a person of ordinary skill in the art at the time of Applicants' invention to copy

the register values and memory contents from one device to the corresponding register values of the other, especially in light of Tzori's explicit teaching of data transfer between the two when re-entering the engaged operating mode.

Regarding claims 4, 5, 15 and 16, these claims are interpreted as meaning that both the microcontroller (DUT) and virtual microcontroller (virtual processor) branch to the beginning of a section of code following a breakpoint (the simultaneously halting step of claim 1). It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to begin a second task at the beginning of that second task upon completion of a first task (boot code or otherwise) when using the system taught by Tzori. Branching to different points in code is extremely well known in the art. If Applicant intends the phrase "branches to assembly instruction line 0" to be read as a literal limitation, clarification is respectfully requested, however the specification (page 28, lines 5-8) appear to teach this phrase as an address stop as known in the art.

Regarding claims 6 and 17, official notice is taken that numerous methods of achieving data protection to effectively "hide data" are well known in the art. It would have been obvious to a person of ordinary skill in the art to hide the boot code from the virtual microcontroller to achieve the numerous advantages of data protection, many of which are known in the art.

Regarding claims 7 and 18, these claims recite setting and initiating a breakpoint, as defined above and known in the art. Official notice is taken that breakpoints are well known in the art. It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to implement breakpoints as known in the art.

Claims 8 and 19 recite combinations of the limitations found in claims 2-4 and 7; and 13-15 and 18, respectively. As these claims are obvious in view of Tzori, as set forth above, different combinations of these limitations are similarly obvious in view of Tzori.

Claims 9 and 20 recite removing a breakpoint. Official notice is taken that removing a breakpoint is well known in the art. It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to remove a breakpoint if he no longer wanted execution to break at that instruction.

Claim 10 recites a combination of limitations found in claims 1, 8, and 9. As these claims are obvious in view of Tzori, as set forth above, different combinations of these limitations are similarly obvious in view of Tzori.

Claim 11 recites a combination of limitations found in claims 1, 8, and 9, as represented in claim 10, and further the limitations of claim 6. As these claims are

obvious in view of Tzori, as set forth above, different combinations of these limitations are similarly obvious in view of Tzori.

6. Claim 21 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Tzori as applied to claim 12 above, and further in view of "Emulation of the Sparcle Microprocessor with the MIT Virtual Wires Emulation System" by Matthew Dahl, Jonathan Babb, Russel Tessier, Silvina Hanono, David Hoki, and Anant Agarwal (Dahl) and further in view of "A Reconfigurable Logic Machine for Fast Event-Driven Simulation" by Jerry Bauer, Michael Bershteyn, Ian Kaplan, and Paul Vyedin (Bauer).

Tzori teaches that the simulation process (virtual processor) is implemented on a Sun workstation (column 6, line 63-65). Tzori does not explicitly teach that the simulation process is implemented on a field programmable gate array (FPGA).

Dahl teaches that it is known in the art to emulate a Sparc microprocessor using an FPGA (abstract).

Bauer teaches that hardware emulation can increase simulation speed by up to 10,000 times (introduction, paragraphs 1-2).

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine these teachings and arrive at the decision to implement the simulation process of Tzori, originally implemented on a Sun workstation, on an FPGA to realize an enormous increase in simulation speed. Knowledge that this was possible is provided by Dahl, and motivation is provided by Bauer.

Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (571) 272-3716. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3713.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jsp

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